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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte WEI-JEN HUANG, CHIH-TSUNG HUANG, SACHIN AGARWAL, and SHA MA

Appeal 2015-006029
Application 12/870,596
Technology Center 2100

Before: HUNG H. BUI, JON M. JURGOVAN, and JOHN R. KENNY, *Administrative Patent Judges*.

KENNY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from rejections of claims 1–6, 12–16, 22, and 23. Final Act. 1; App. Br. 13. Claims 7–11, 17–21, and 24–26 have been withdrawn from consideration. Final Act. 1. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE and enter NEW GROUNDS OF REJECTION.

CLAIMED INVENTION

The claimed invention relates to memory management techniques. Spec. ¶ 1. Claims 1 and 6, reproduced below with their disputed limitations italicized, are illustrative of the claimed subject matter:

> 1. A method for performing multiple write operations in parallel, comprising:
>
> during a first read/write cycle, performing a first write operation by writing data to a first memory address in a first block of addresses, wherein the first block is one of a plurality of blocks; and
>
> *in parallel to performing the first write operation, during the first read/write cycle, performing a second write operation by writing data for a second memory address in the first block of addresses to a pending write queue/cache.*
>
> 6. A method, comprising:
>
> during a first read/write cycle, performing a first read operation by reading data from one of (i) a pending write queue/cache if the read data is determined to be in the pending write queue/cache or (ii) a first memory address in a first block of addresses, wherein the first block is one of a plurality of blocks, if the read data is determined to not be in the pending write queue/cache; and
>
> *in parallel to performing the first read operation, performing a first write operation by writing data for a second memory address in the first block of addresses to the pending write queue/cache located in memory, in response to determining (i) the read data and the write data are in the first block of addresses and (ii) the first read data is determined to not be in the pending write queue/cache.*

App. Br. 15 (Claims Appendix) (emphasis added).

REFERENCES

Kim US 2006/0020764 A1 Jan. 26, 2006

Jun Shao & Brian T. Davis, *A Burst Scheduling Access Reordering Mechanism*, IEEE, 285–94 (2007) ("Shao").

REJECTIONS

(1) Claims 1, 2, 12, 13, 22, and 23 stand rejected under 35 U.S.C. § 102(b) as anticipated by Kim. Final Act. 3.

(2) Claims 3–6 and 14–16 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Kim and Shao. Final Act. 4.

ANALYSIS

Claims 1, 2, 12, 13, 22, and 23

Appellants argue that Kim does not disclose the disputed limitation: "in parallel to performing the first write operation, during the first read/write cycle, performing a second write operation by writing data for a second memory address in the first block of addresses to a pending write queue/cache" as recited in independent claim 1, and similarly recited in independent claims 12 and 22. App. Br. 8–12; Reply Br. 2–4. In particular, Appellants and the Examiner dispute whether a write operation involving the second command in Kim occurs in parallel with a write operation involving the first command. App. Br. 8–12; Ans. 2–5; Reply Br. 2–4. Figure 7 of Kim, reprinted below, specifies the write operations-at-issue:

Fig. 7

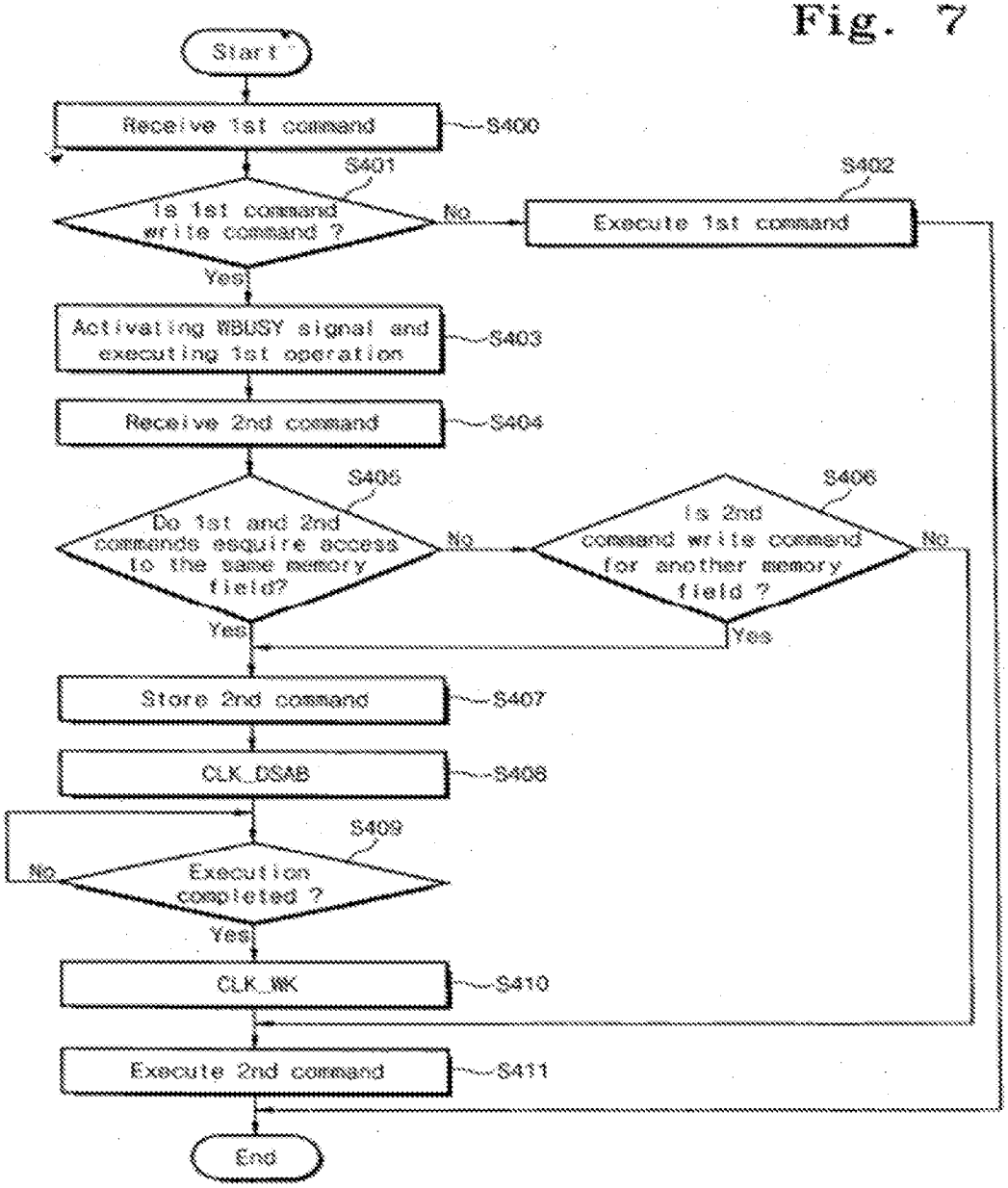

Figure 7 of Kim.

Appellants note that the write operation in step 411 is not performed in parallel with the first write operation because step 411 occurs after step 409, where the first write operation is completed. App. Br. 8–12; Reply Br. 2–4. The Examiner finds earlier steps in Kim's Figure 7 meet the limitation. Ans. 2–5.

The earlier step in Kim's Figure 7 that involves writing with the second command is step 407. In describing step 407, Kim, however, does not expressly disclose writing data for the second memory address (rather than just the write command itself) to the pending write queue/cache, and the Examiner does not explain how Kim implicitly or inherently discloses the writing of such data in that step (or in any of the other steps prior to step 409). *Id.* at ¶ 80, Fig. 7; Ans. 2–5. Accordingly, we do not sustain the Examiner's anticipation rejection of independent claims 1, 12, and 22 and their respective dependent claims 2, 13, and 23.

Pursuant to our authority under 37 C.F.R. § 41.50(b), however, we enter a new ground of rejection for independent claims 1, 12, and 22, and dependent claims 2, 13, and 23, rejecting these claims as unpatentable under 35 U.S.C. § 103(a) over the combination of Kim and U.S. Patent No. 8,250,328 B2 to Farrell et al., issued August 21, 2012 ("Farrell"). Farrell is prior art to the pending application under 35 U.S.C. § 102(e). Farrell was filed on March 24, 2009, whereas the pending application was filed on August 27, 2010. Farrell (22); Final Act. 1; App. Br. 1; Combined Declaration and Power of Attorney, filed August 27, 2010, p. 2; September 10, 2010 Filing Receipt, p. 1. Farrell is also analogous art. *See* Spec. ¶ 1, Farrell Abstract, Technical Field.

Kim's description of step 407 teaches or suggests part of the disputed limitation. In particular, that step teaches or suggests, in parallel to performing the first write operation, during the first read/write cycle, writing a second write command for writing data for a second memory address in the first block of addresses to a pending write queue/cache. Kim ¶ 80, Fig. 7. Specifically, in step 407, the second write command is latched (i.e., stored) to flip-flop circuit 150. *Id.* Later, in step 411, that command is read

and executed, meaning flip-flop circuit 150 is a pending write que/cache. *Id.* at ¶ 83, Fig. 7. Kim teaches or suggests performing step 407 in parallel to Kim's first write operation because step 407 occurs after step 403, where the first write operation is stated to be executing, and before step 409, in which the execution of the first command is completed. *Id.* at ¶¶ 80–81, Fig. 7. Farrell discloses buffering the data for write commands along with the write commands. Farrell 4:58–5:11.

Because Kim does not specify what to do with the data that is to be written by a queued write command (*see* Kim ¶ 80), and Farrell expressly teaches that such data can be buffered with the write command, we find an ordinarily skilled artisan would recognize that incorporating Farrell's teaching into Kim's system would permit data to be more accessible when executing the buffered write command. Farrell 4:58–5:11.

Accordingly, we newly reject independent claims 1, 12 and 22 and dependent claims 2, 13, and 23, not separately argued, for obviousness over the combination of Kim and Farrell. App. Br. 8–12. For this new rejection, we adopt the Examiner's findings and rationales set forth in the Final Office Action and the Examiner's Answer for those claims, except as otherwise noted above.

Claims 3–5 and 14–16

Claims 3–5 and 14–16 each depend from independent claims 1 and 12 respectively. Accordingly, we also do not sustain the rejection of claims 3–5 and 14–16, and pursuant to 37 C.F.R. § 41.50(b), we newly reject those claims as unpatentable under 35 U.S.C. § 103(a) over the combination of Kim, Shao, and Farrell. (*See* discussion above regarding the disputed limitation of claim 1.) Appellants do not challenge the Examiner's findings regarding the limitations added by claims 3–5 and 14–16. App. Br. 13. For

our new rejection, we adopt the Examiner's findings and rationales set forth in the Final Office Action and the Answer for claims 3–5 and 14–16 and the claims from which they depend, except as otherwise noted above.

Claim 6

Appellants argue that the combination of Kim and Shao does not teach or suggest the disputed limitation in claim 6. App. Br. 12–13; Reply Br. 5. Appellants present essentially the same arguments they presented for disputed limitation of claim 1, which are applicable to the disputed limitation of claim 6. App. Br. 12–13; Reply Br. 5. Therefore, we do not sustain the rejection of claim 6, and pursuant to 37 C.F.R. § 41.50(b), we newly reject claim 6 as unpatentable under 35 U.S.C. § 103(a) over the combination of Kim, Shao, and Farrell. (*See* discussion above regarding the disputed limitation of claim 1.) For our new rejection, we adopt the Examiner's findings and rationales set forth in the Final Office Action and the Answer for claim 6, except as otherwise noted above.

DECISION

We reverse the rejections of claims 1–6, 12–16, 22, and 23.

Pursuant to 37 C.F.R. § 41.50(b), we newly reject:

(i) claims 1, 2, 12, 13, 22, and 23 as unpatentable under 35 U.S.C. § 103(a) over the combination of Kim and Farrell; and

(ii) claims 3–6 and 14–16 as unpatentable under 35 U.S.C. § 103(a) over the combination of Kim, Shao, and Farrell.

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b). Section 41.50(b) provides "[a] new ground of rejection pursuant

to this paragraph shall not be considered final for judicial review." Section 41.50(b) also provides:

> When the Board enters such a non-final decision, the appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:
>
> > (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground of rejection is binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground of rejection designated in the decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.
> >
> > (2) *Request rehearing.* Request that the proceeding be reheard under §41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to a new ground of rejection can be found in the *Manual of Patent Examining Procedure* § 1214.01 (9th Ed., Rev. 07.2015, Nov. 2015).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED; 37 C.F.R. § 41.50(b)